Working Group Goals : Overall

- Identify and prioritize the top challenges for your WG as it pertains to building an Exaflop scale supercomputer in the 2015-18 timeframe
- Background information on applications, programming models used by DOE, and sketches of Exascale system configurations
- Expect a 'top 10' list for your 2-3 page section of the final report

System Interconnects

	2011		2015		2019	
System Size Sockets Peak PF TF/Socket	32,768 32 1.0		32,768 200 6.1		32,768 800 25.0	
	Expect	Want	Expect	Want	Expect	Want
NIC B/W (B/F)	0.01 - 0.1	1.0	0.005 - 0.03	1.0	0.025 - 0.25	1.0
Link B/W (B/F)	0.01 - 0.1	1.0	0.005 - 0.03	1.0	0.025 - 0.25	1.0
MPI Latency (ns)	750 - 1500	500	500 - 1000	400	400 - 750	300
MPI Throughput (M Msg/s)	20	50	80	300	300	1200
Load/Store (M Msg/s)	75	400	150	1,600	300	6400
Load/Store Latency (ns)	300	100	300	100	300	100

Sandia National Laboratories

Recommended Dimensions for Prioritization

- **<u>Probability</u> that the challenge will not be solved by relying on current technology trends: high, med, low**
- **<u>Impact</u> that the lack of a solution for this challenge will have on the ability of the HPC community to build an exascale computer by 2016: high, med, low**
  - That is, HIGH means that if we don't have a solution for this problem, there is no workaround solution that will allow us to build the exascale system
- **Approximate NRE <u>cost</u> for a solution: high (greater than $15M), med ($5-10M), low (less than $5M)**
- **Strategic non-technical challenges**
  - Keep separate list

Working Group Deliverables

- **For each topic**
  - Current Status
  - Exascale Requirements
  - Findings
- **Challenges**
  - Ordered List of Priorities
  - Impact
    - High, medium, low
  - Probability
    - High, medium, low
  - Cost
    - High, medium, low
  - Slightly different for device technology panel
- **You have ~3 hours**
- **WG chairs have organized**
- **WG chairs have been asked to keep the conversations on track**
  - Don't be offended
- **Divide and conquer if necessary**
- **Don't try to solve the technical problems per se**
- **Participate**

Factors

- **Performance**
  - Bandwidth, latency, messaging rate, application performance
- **Power**
- **Reliability, Resilience**
- **Scalability**
- **Manufacturability**
- **Cost**

Device and Emerging Technologies WG

- **Metrics for interconnect technologies**
  - Cost/bit/sec
  - Energy/bit
  - Density (bits/sec, per chip, etc.)

Interconnect domains

- On-chip (mm-cm)
- On-module (cm)
- On board (20cm)
- Intra-cabinet (0.5-1m)
- Inter-cabinet (2-50m)

WG Plan: examine key emerging technologies at multiple domains, evaluate challenges, impact

Key Emerging Technologies

- CMOS
- Silicon Photonics
- Proximity coupling
- MEMS
- Other?

On-chip

- **256 cores, ~10TF, 10TB/s global (2cm)**
- **CMOS**
  - > 1 pJ/bit (across 2cm wire) ~80W
  - > Aggressive scaling of CMOS, no exotic technologies, etc.
  - > (note – calculate system level – 8W/F…)

Emerging technologies

- **CMOS**
  - > Traditional electrical channels
    - – 15pJ/bit
  - > Packaging, cooling
  - > SERDES
    - – Challenges: size scaling, power dissipation
  - > Opportunities:

- **10pJ/Flop**
- **128 F of energy to read word DRAM**