

# Three-Dimensional Integrated Circuits

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# Presentation Outline

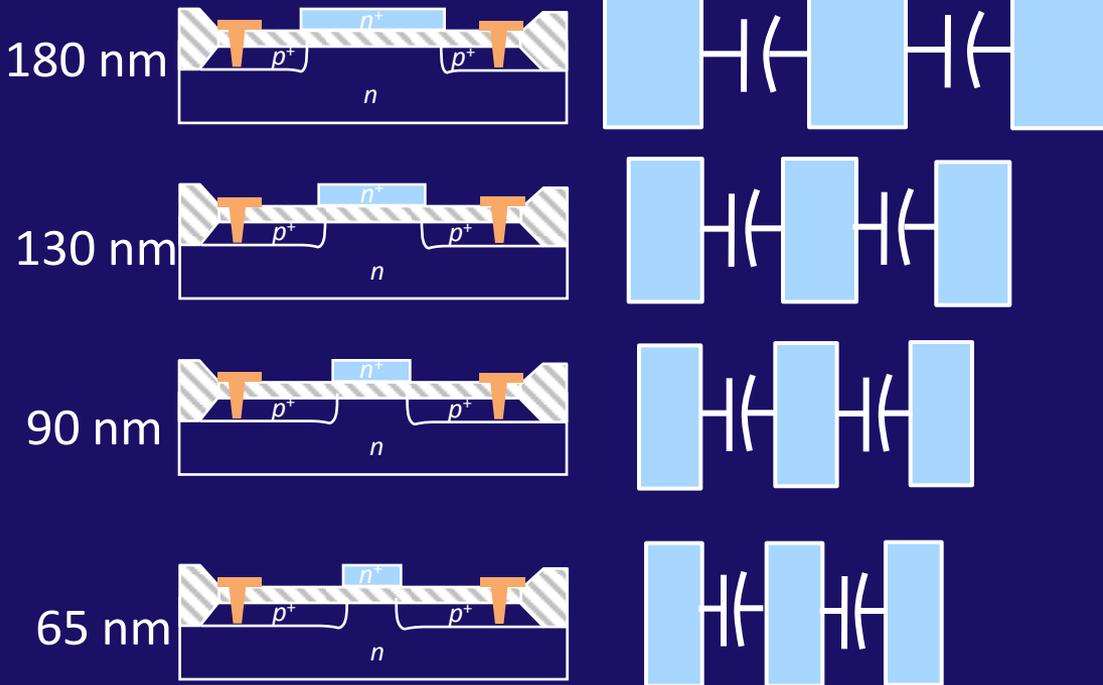
- Three-dimensional (3-D) integration
- Physical design issues in 3-D integration
- 3-D Networks-on-chip
- Synchronization in 3-D circuits
- Conclusions

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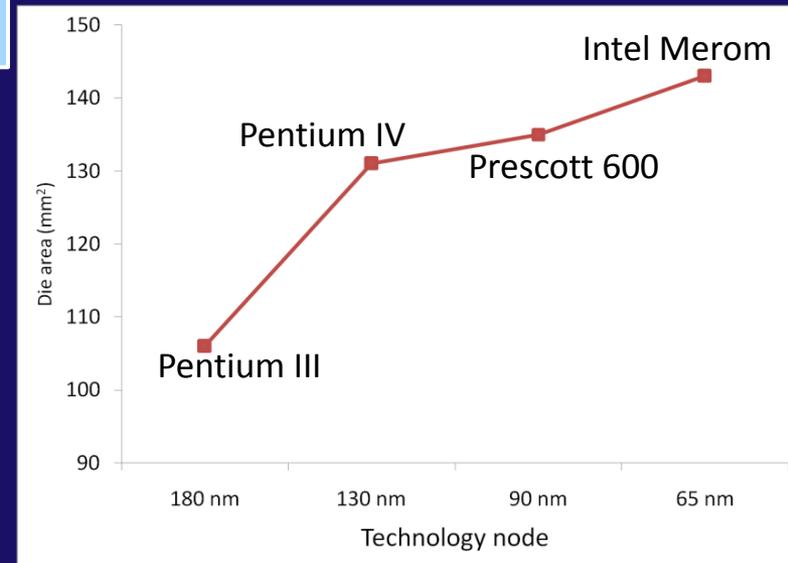
- Three-dimensional (3-D) integration
  - Limitations of modern ICs
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# Scaling Issues in Modern ICs

- Device scaling
- Global interconnects



- $\mu$ P die area

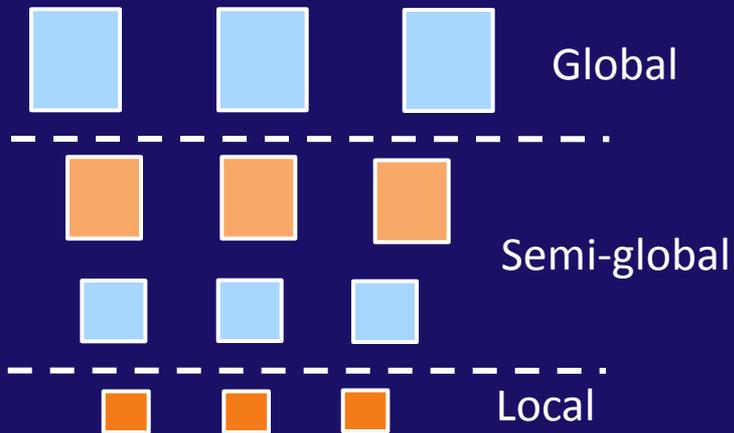
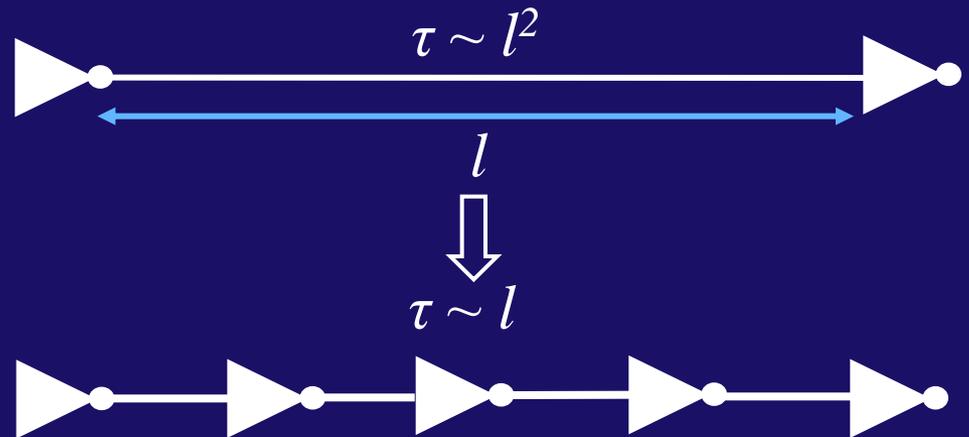
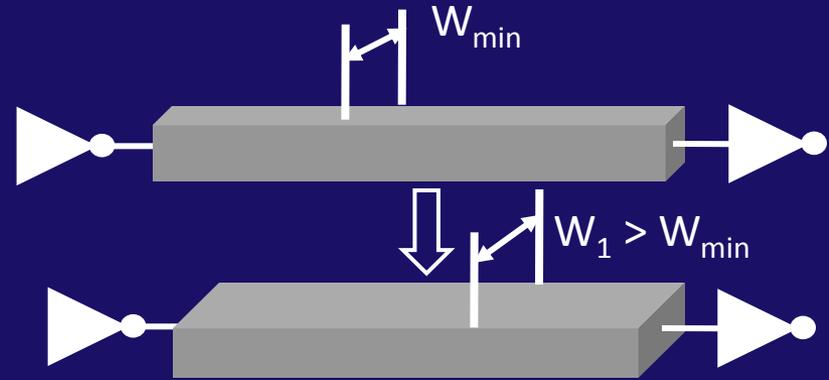


- Device speed increases
- Coupling capacitance increases
- Resistance increases
- $\tau \sim RC$

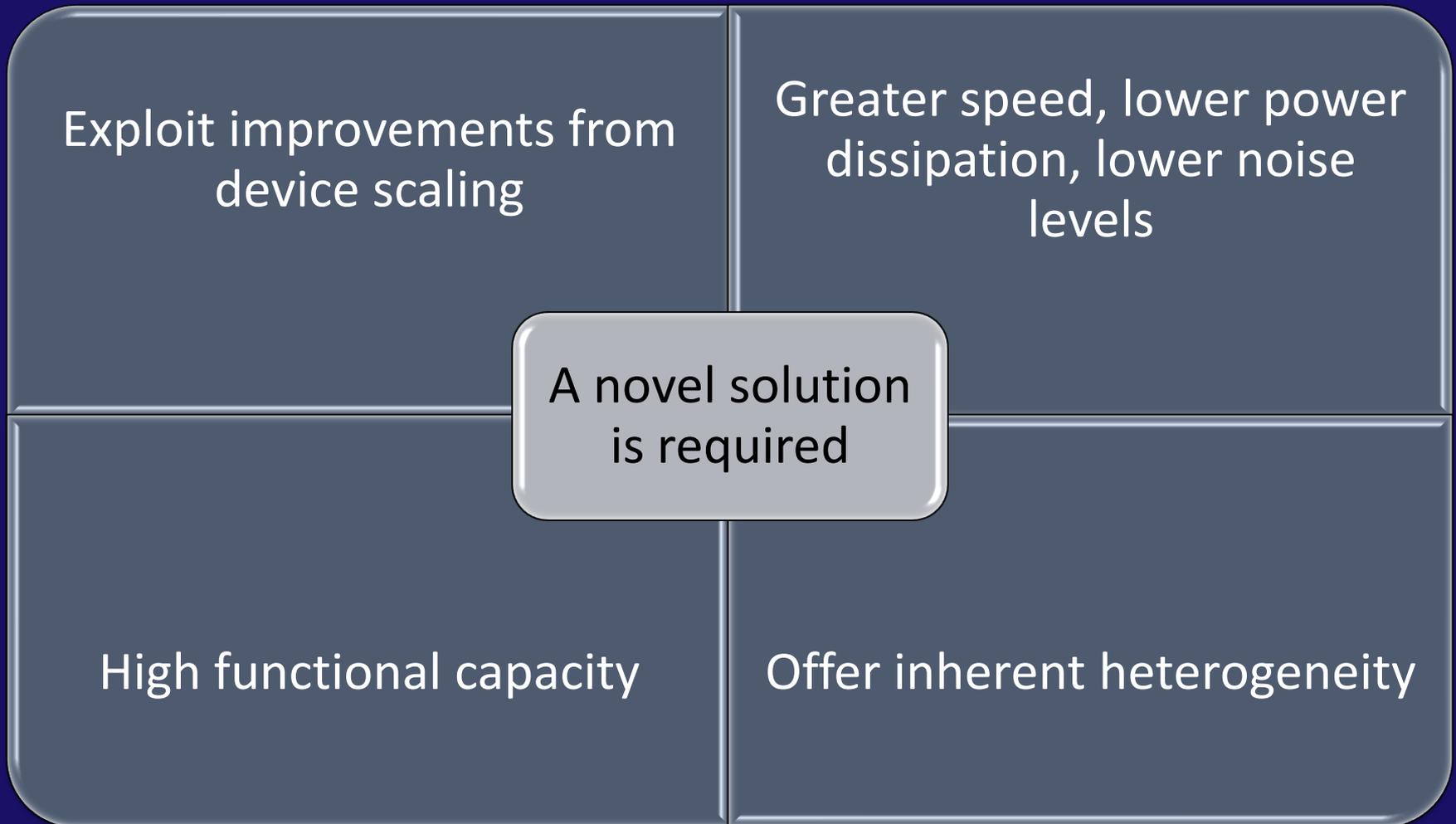
- On-chip interconnect length increases

# Known (But Limited) Design Techniques

- Wire sizing
- Repeater insertion
- Multi-tier interconnect architectures

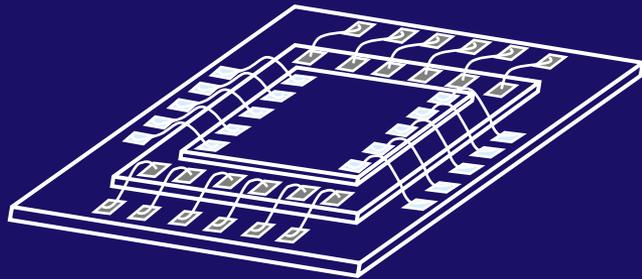


# Break Through the Interconnect Wall

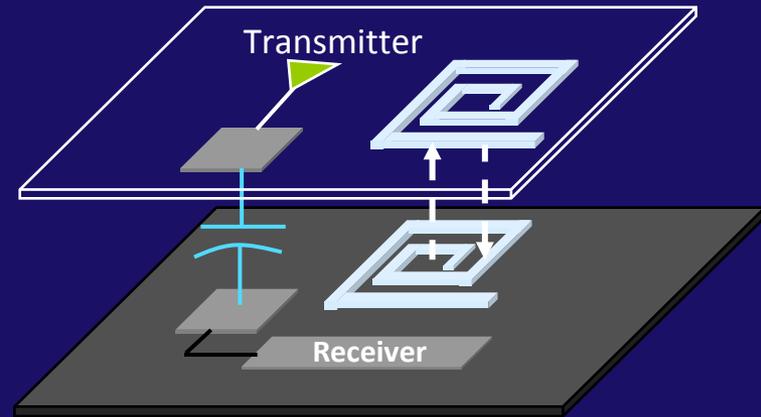


# Forms of 3-D Integration

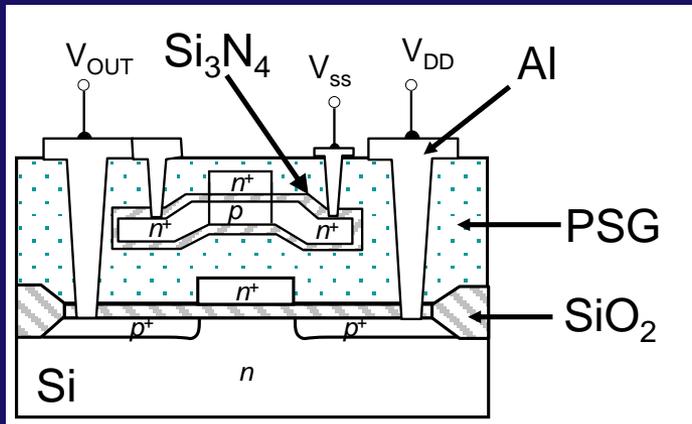
- Wire bonded die



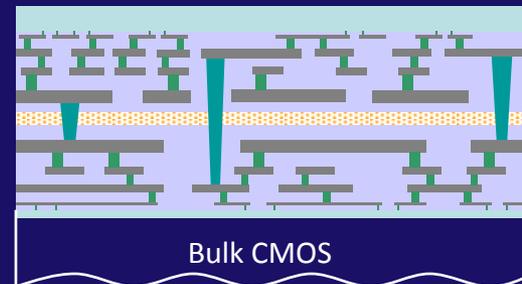
- Contactless 3-D circuits



- Stacked 3-D circuits



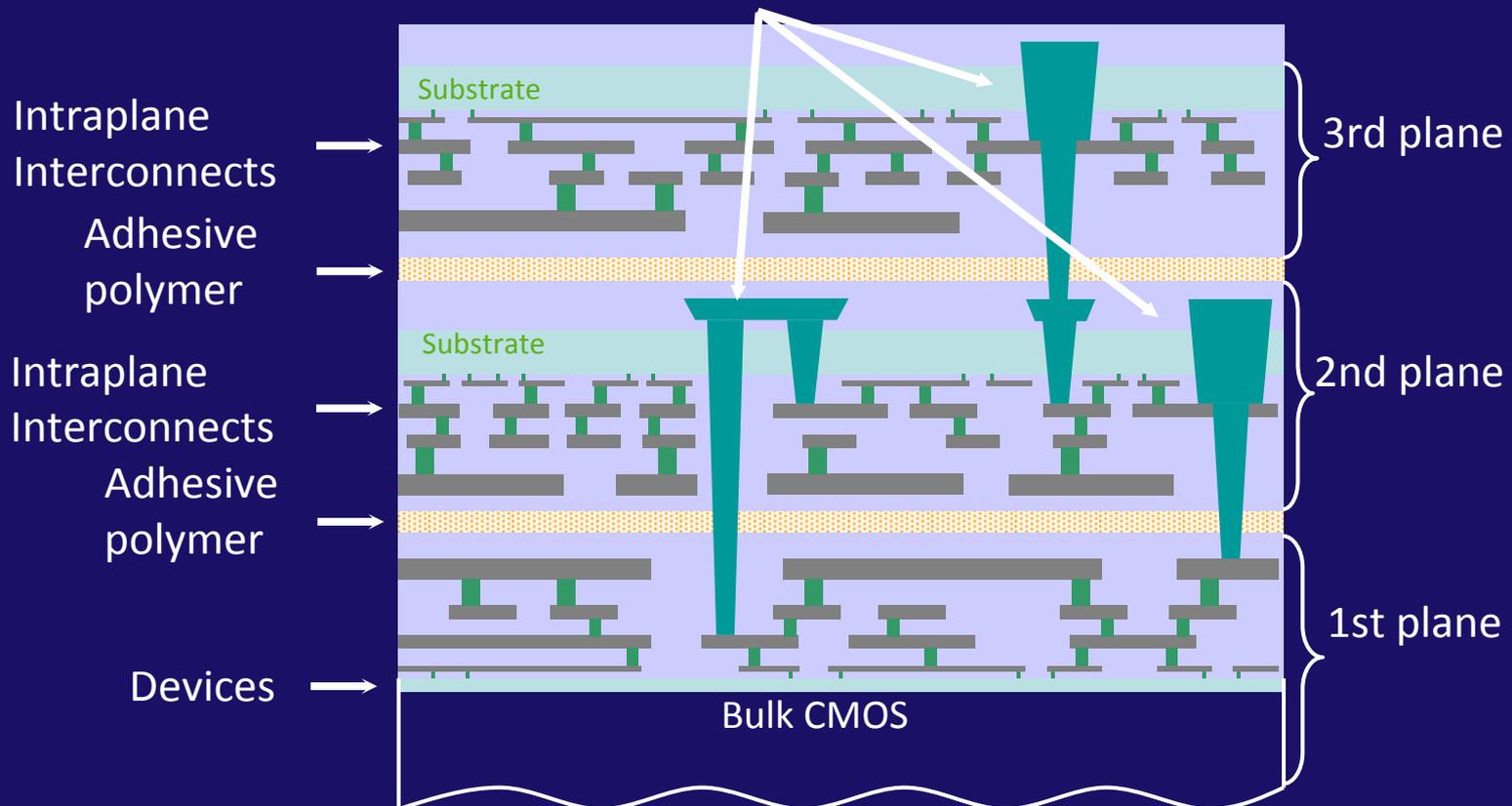
- 3-D ICs – Fine grain interconnects



# Cross-Section of a 3-D Integrated Circuit

- Different plane bonding styles
- Bonding materials
  - Wafer thinning

Through silicon vias (TSV)



\*R. J. Gutmann *et al.*, "Three-Dimensional (3D) ICs: A Technology Platform for Integrated Systems and Opportunities for New Polymeric Adhesives," *Proceedings of the Conference on Polymers and Adhesives in Microelectronics and Photonics*, pp. 173-180, October 2001

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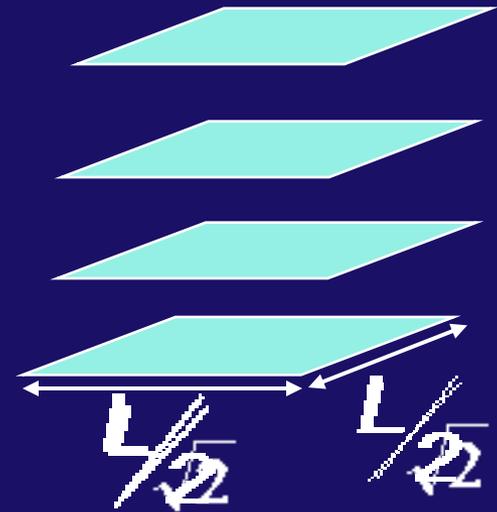
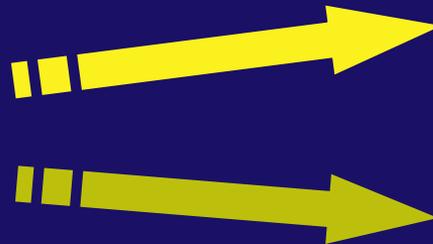
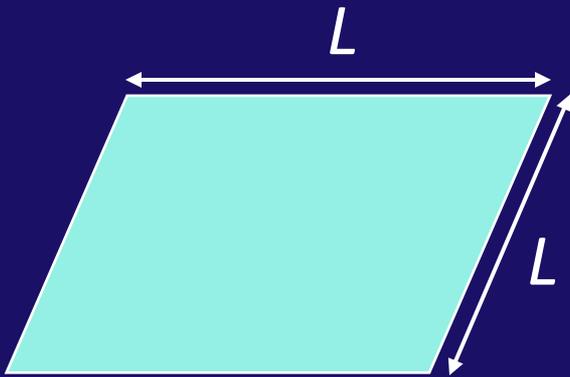
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# 3-D Integration

Maximum wirelength reduction

2 planes ~30%

4 planes ~50%

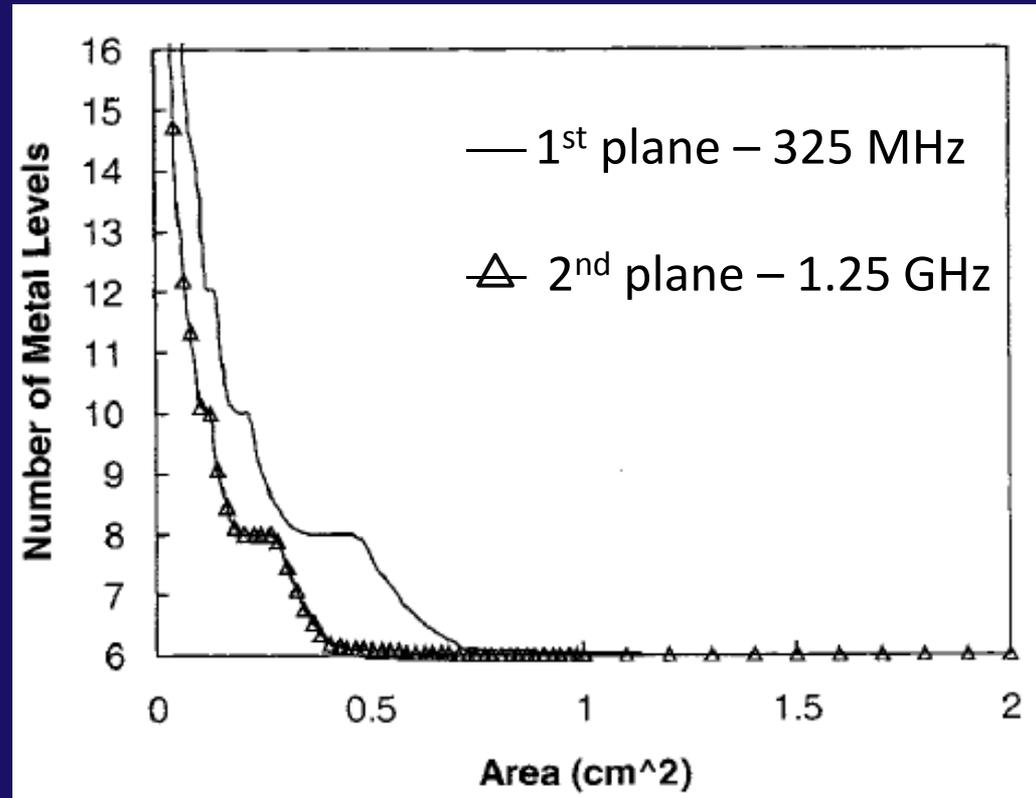


- Area =  $L^2$
- *Corner to corner distance* =  $2L$

- Area =  $L^2$
- *Corner to corner distance*  $\approx \sqrt{2}L$

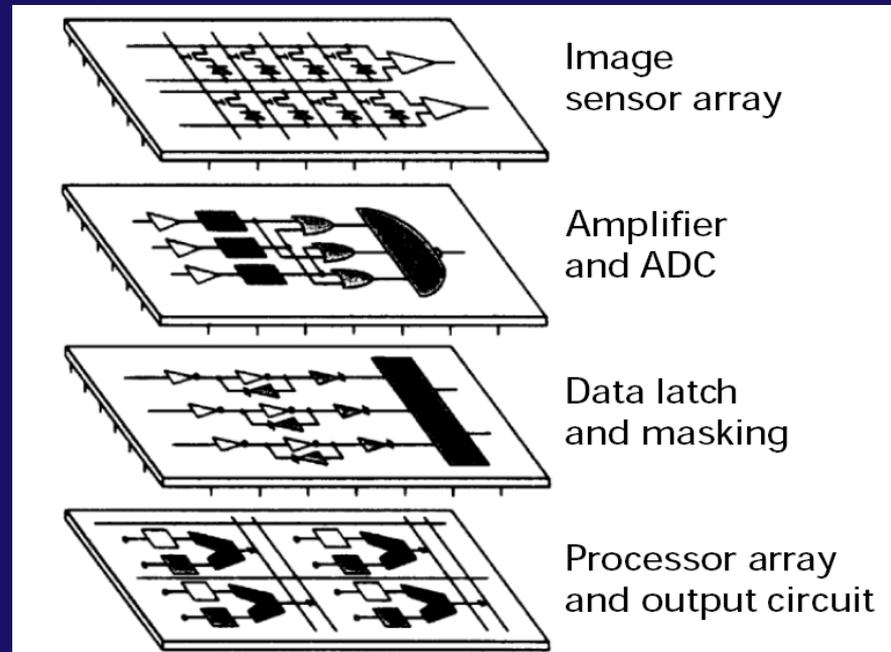
# Advantages of 3-D Integration

- Higher performance
  - Speed and power
- Area reduction
  - For wire-limited circuits
    - Fixed clock frequency
- Decrease in interconnect resources
  - Number of metal layers
    - For specific speed and area



# Heterogeneous 3-D Systems-on-Chip

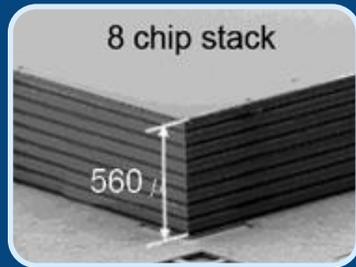
- Real time image processing system
- Integration of
  - Circuits from different fabrication processes
  - Non-silicon technologies
  - Non-electrical systems



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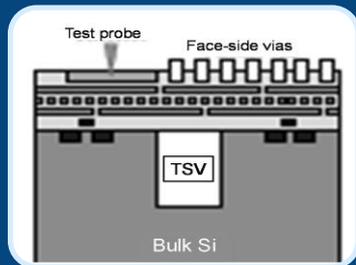
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# Spectrum of Challenges in 3-D ICs



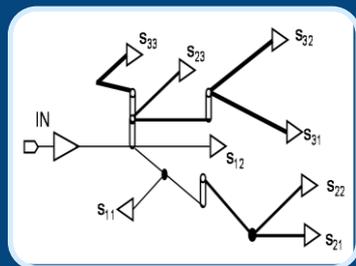
## Manufacturing

- Plane alignment and bonding
- Through silicon vias



## Testing

- Pre-bond testing
- Post-bond testing



## Design

- Interconnect design techniques
- Thermal management techniques
- Physical design techniques

# Objective for 3-D CAD Tools

“New design tools will be required to optimize interlayer connections for maximized circuit performance...”

## TSVs

- Density / consume silicon area
- Impedance characteristics

## Heterogeneity

- Interdie process variations
- Disparate technologies

## Interconnect length

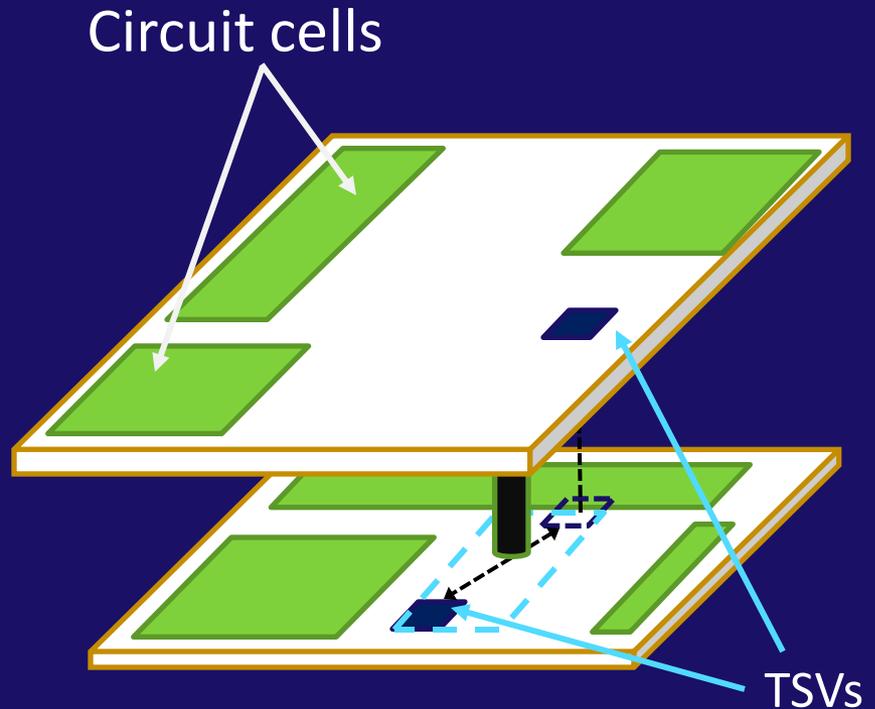
- Longest nets in a 3-D system

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# Through Silicon Via Placement Approaches

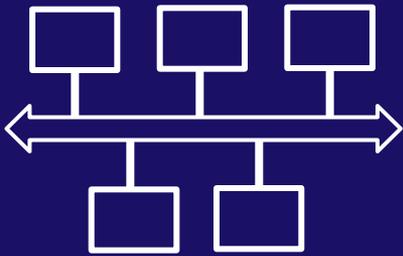
- Treat TSVs as circuit cells
  - Use weighted average distance to determine final via location
- Place the cells of each plane separately
  - Including vias



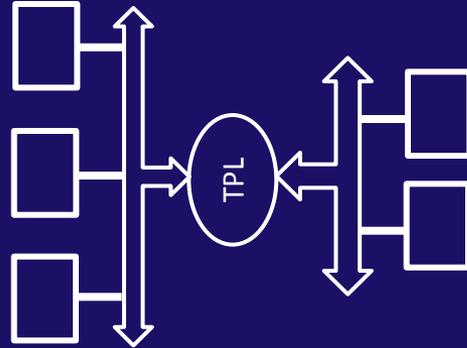
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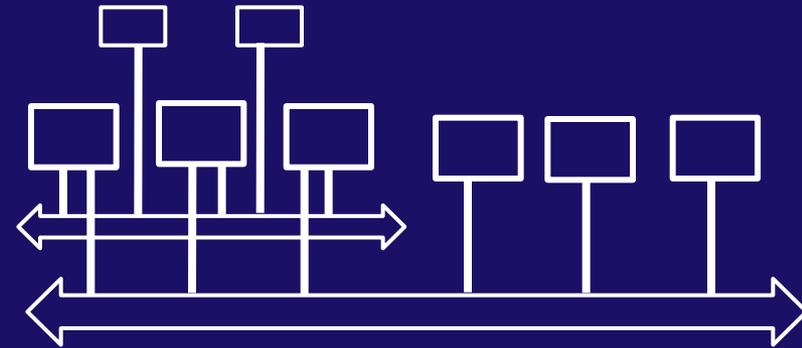
# Evolution of Interconnect Architectures



- Shared buss

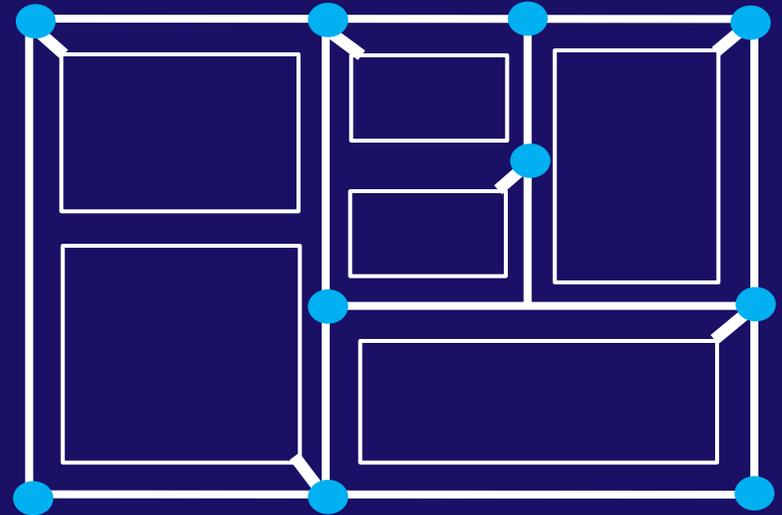


- Segmented buss



- Multi-level segmented buss

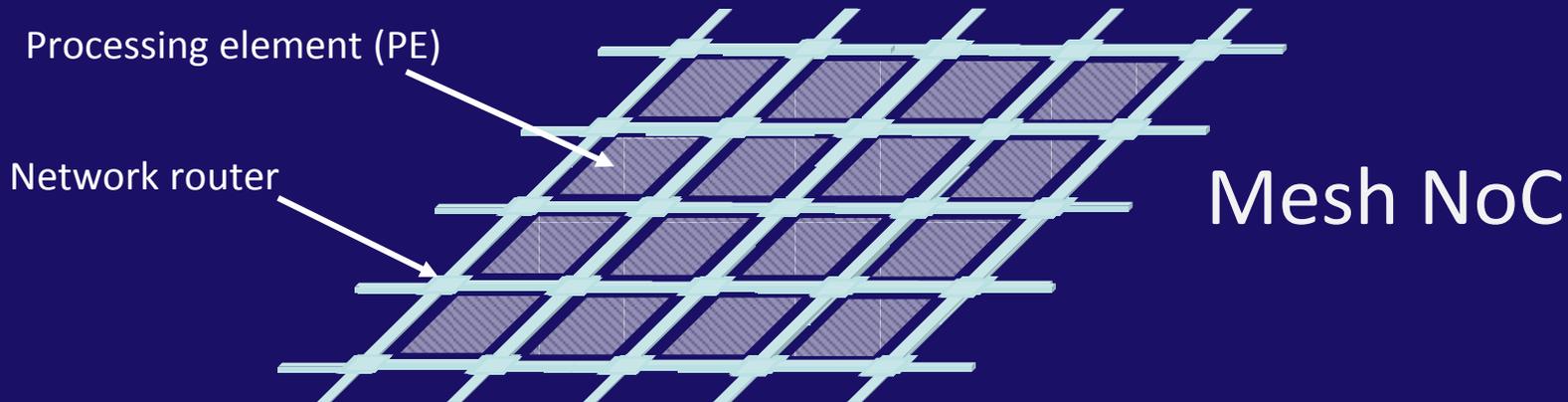
- Buss architecture limitations
  - Large buss delays
  - Data contention for resources
  - Signal integrity



- Network-on-chip

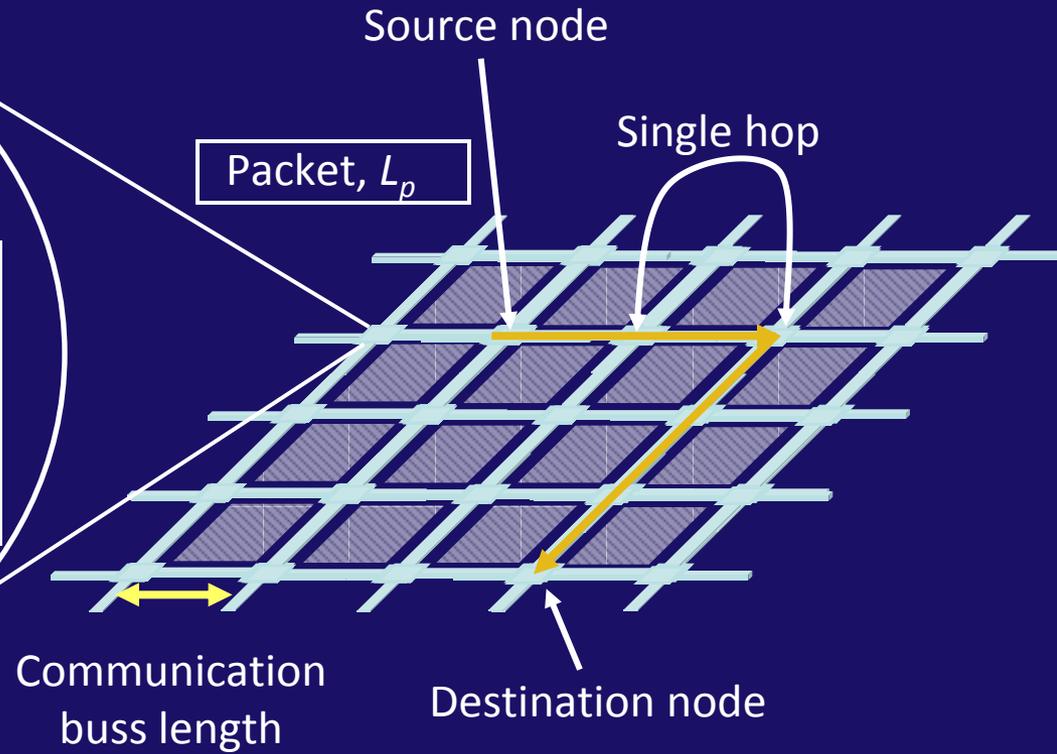
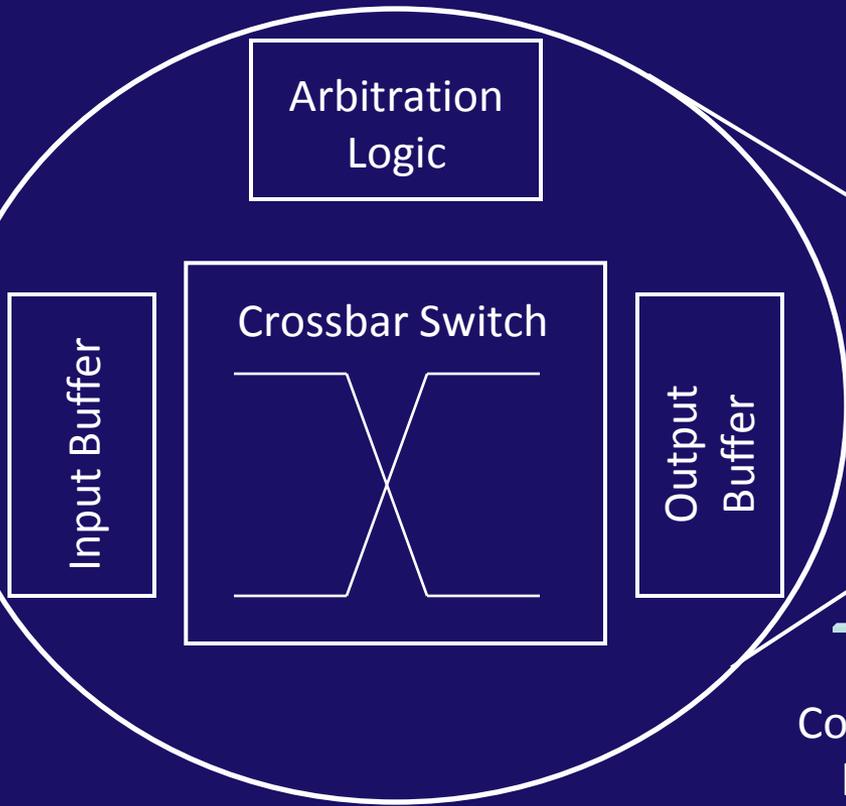
# Network-on-Chip (NoC)

- Network-on-chip is another approach to mitigate the interconnect bottleneck in modern IC design
  - Canonical interconnect structure
  - Shared interconnect bandwidth
  - Increased flexibility
- PEs exchange data packets through the network in an internet-like manner
- Network routers transfer data within the network similar to computer networks

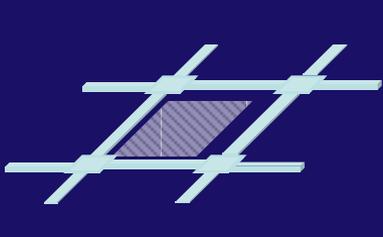
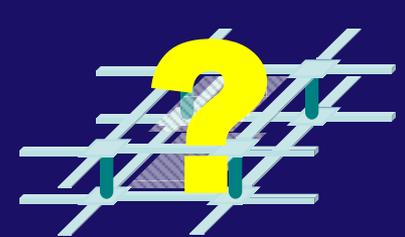
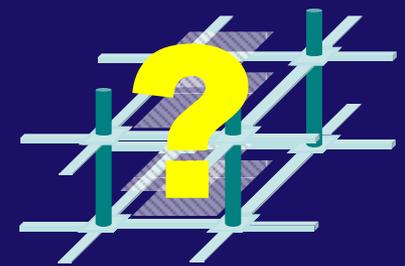


# NoC Mesh Structure

Router



# Various Topologies for 3-D Mesh IC-NoC

IC \ NoC	2-D	3-D
2-D		
3-D		



- Reduced number of hops



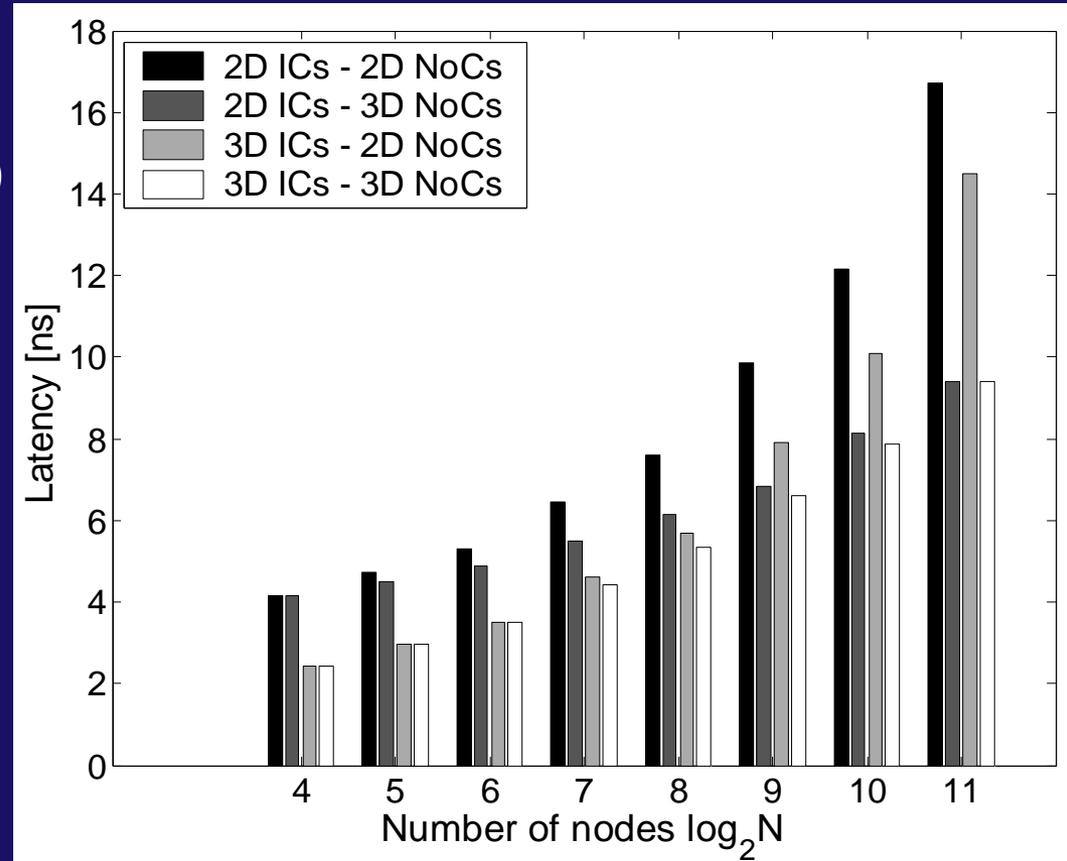
- Reduced number of hops and buss length



- Shorter buss length

# Performance Comparison for 3-D NoC Topologies

- Dense networks with small PE areas favor 3-D NoCs and 2-D ICs
  - Due to large number of hops and short busses
- Small networks with large PE areas favor 3-D IC and 2-D networks
  - Due to small number of hops and long busses



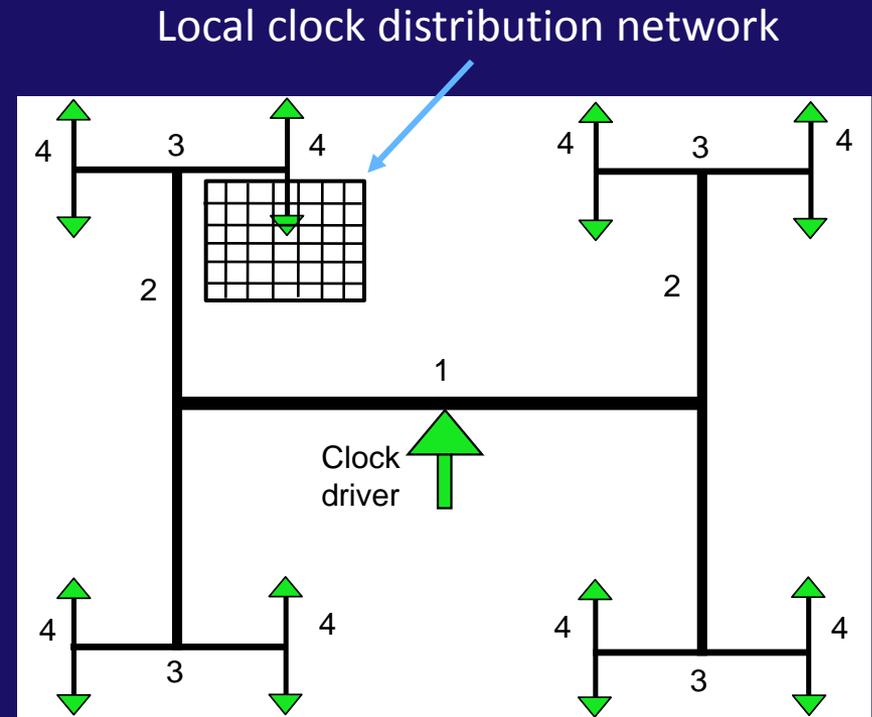
- $A_{PE} = 4 \text{ mm}^2$
- Improvement = 36.2%,  $N = 256$

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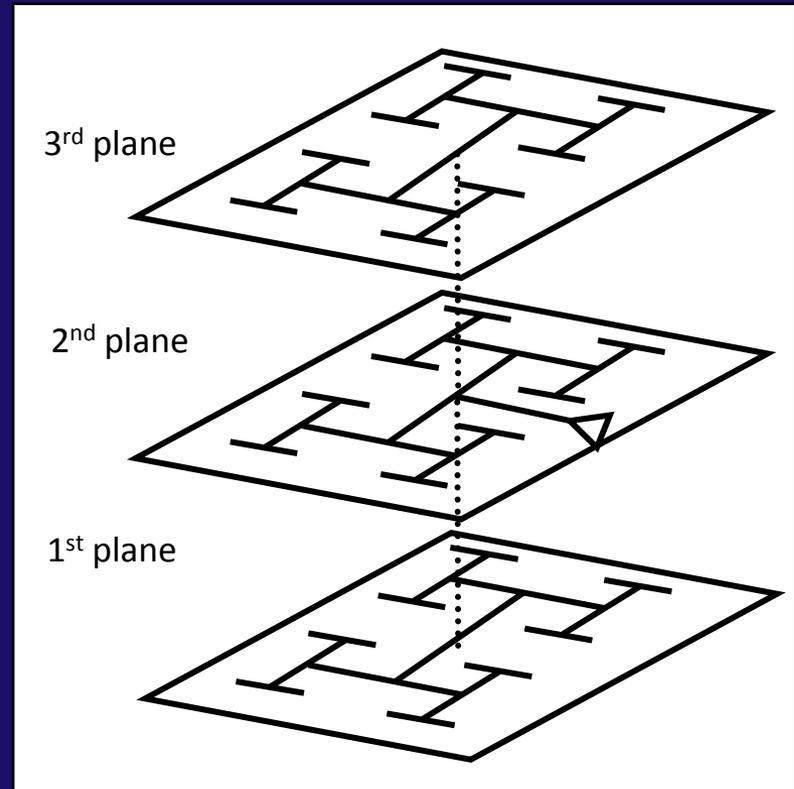
# Clock Distribution Networks

- Clock signal is the “heart” of synchronous circuits
- VDSM technologies
  - Increasing frequencies
  - Greater process variations
  - Clock skew, jitter should be carefully managed
- Hierarchical clock distribution networks
  - Global networks
    - H-tree, X-tree
  - Local networks
    - Meshes



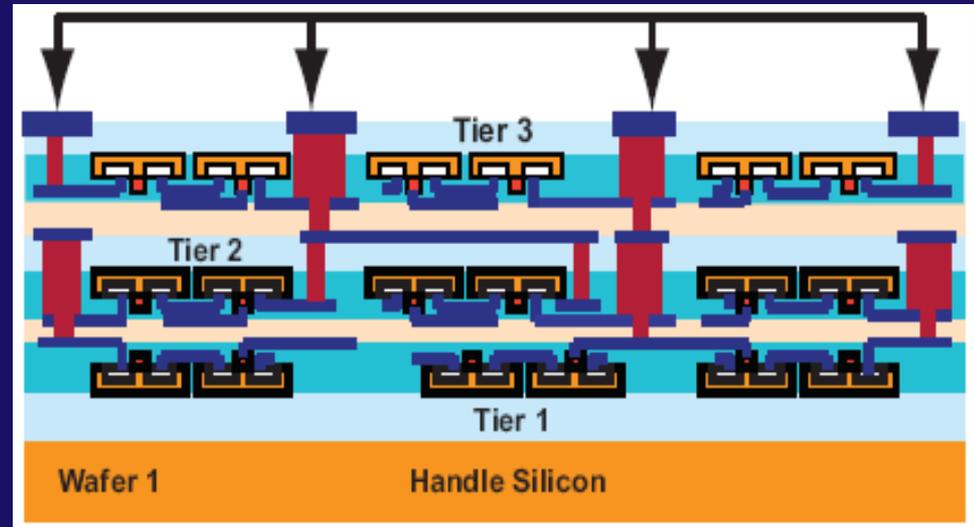
# Clock Signal Distribution for 3-D ICs

- Multiplane system
  - Process variations
- Different forms of 3-D integration
  - System-in-Package (SiP)
  - 3-D ICs (high density vias)
- Clock signal distribution under pronounced thermal effects



# MIT Lincoln Laboratories 3-D IC Fabrication Process

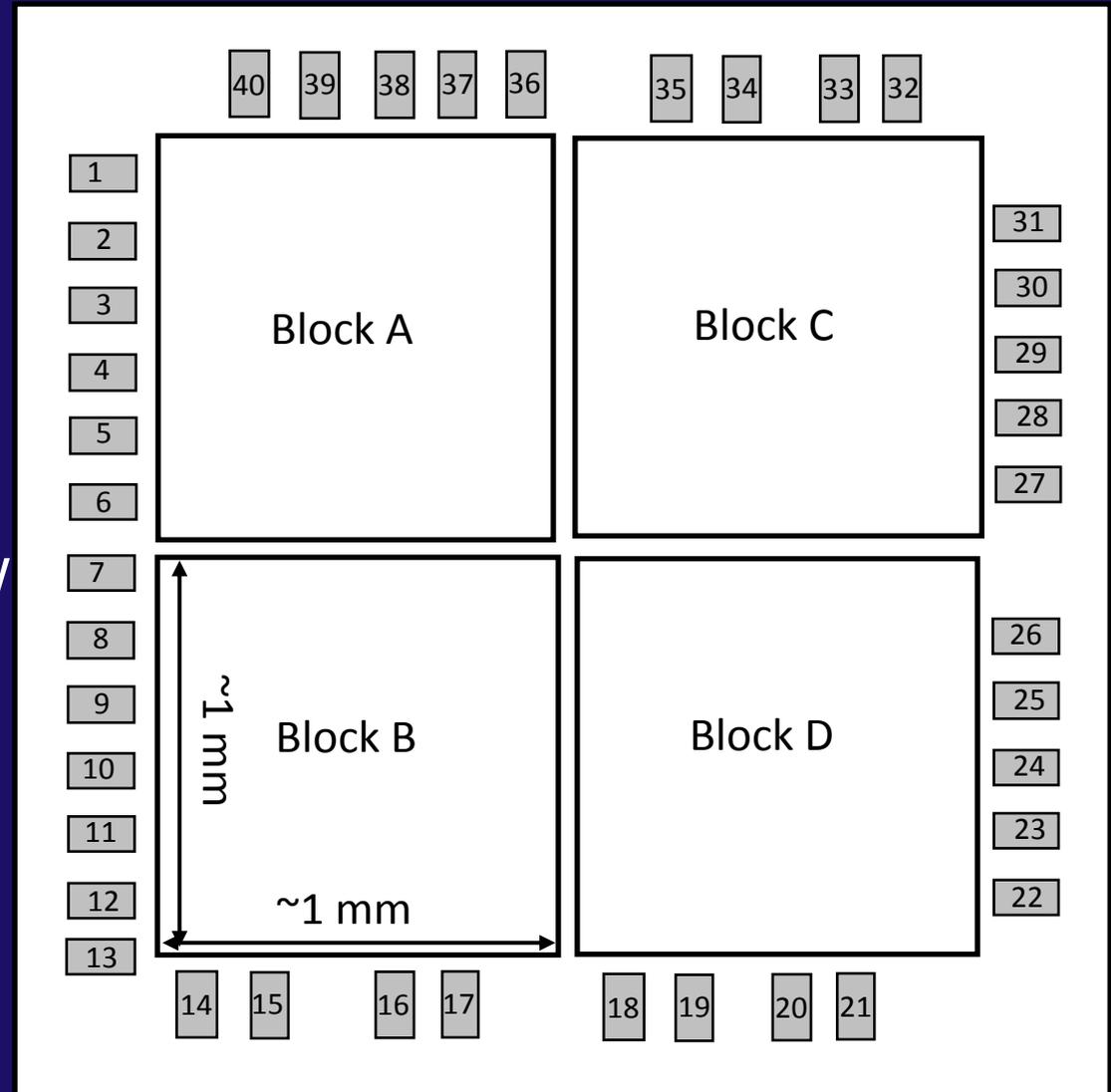
- FDSOI 180 nm CMOS process
  - Three plane process
  - Three metal layers for each plane
  - Back side metal layer for planes 2 and 3
  - One polysilicon layer
- $1.75 \mu\text{m} \times 1.75 \mu\text{m}$  cross section of TSVs



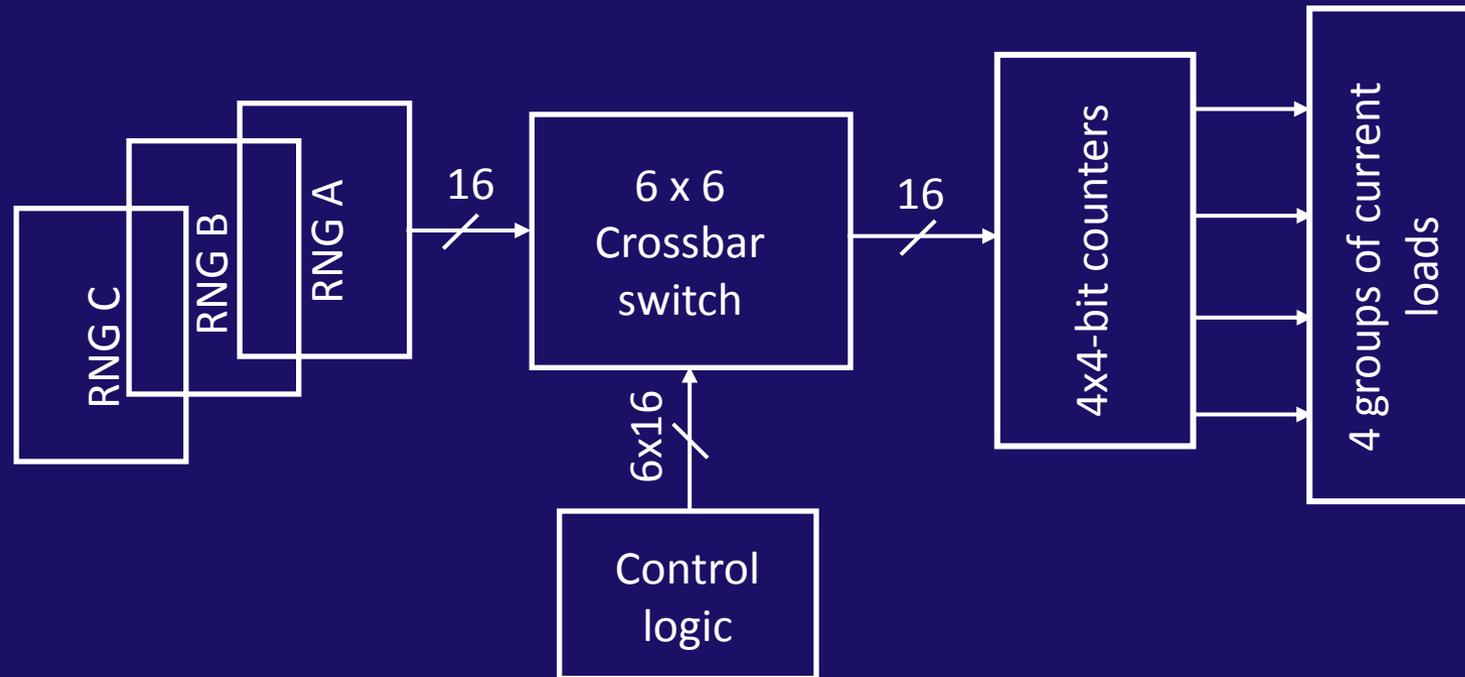
- Planes one and two
  - Face to face bonding
- Planes two and three
  - Back to face bonding

# Block Diagram of the 3-D Test Circuit

- Each block includes
  - Identical logic
  - Different clock distribution network
- Objectives
  - Evaluate clock skew
  - Measure power consumption
- Area - 3 mm × 3 mm

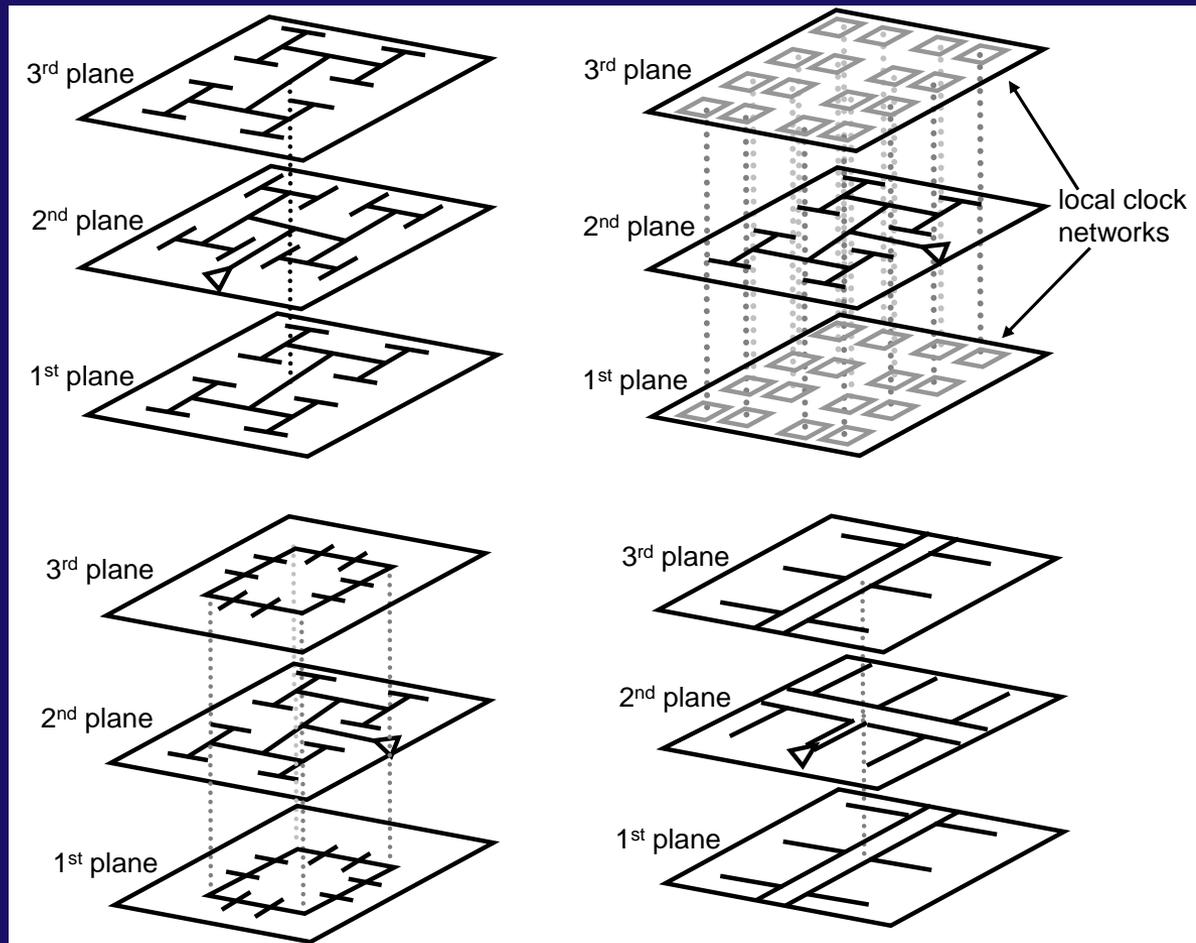


# Logic Circuitry



- Current loads mimic various switching patterns
- Control logic periodically changes the connectivity among the input and output ports

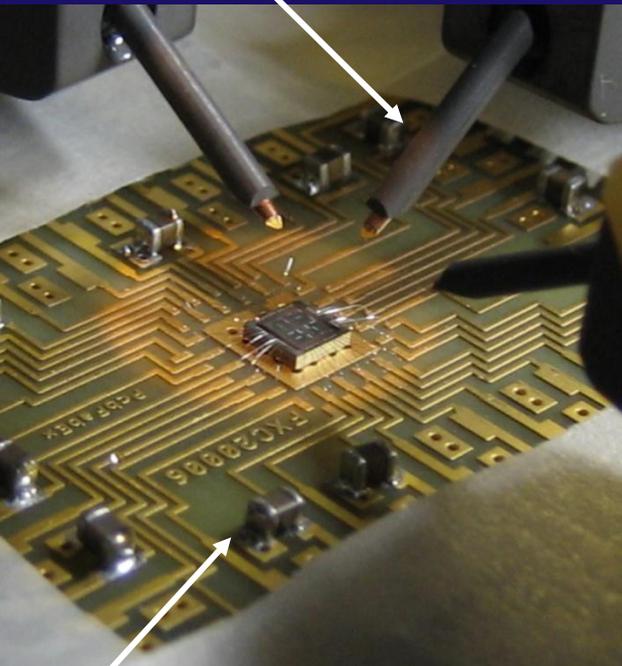
# Explored Clock Distribution Networks for 3-D ICs



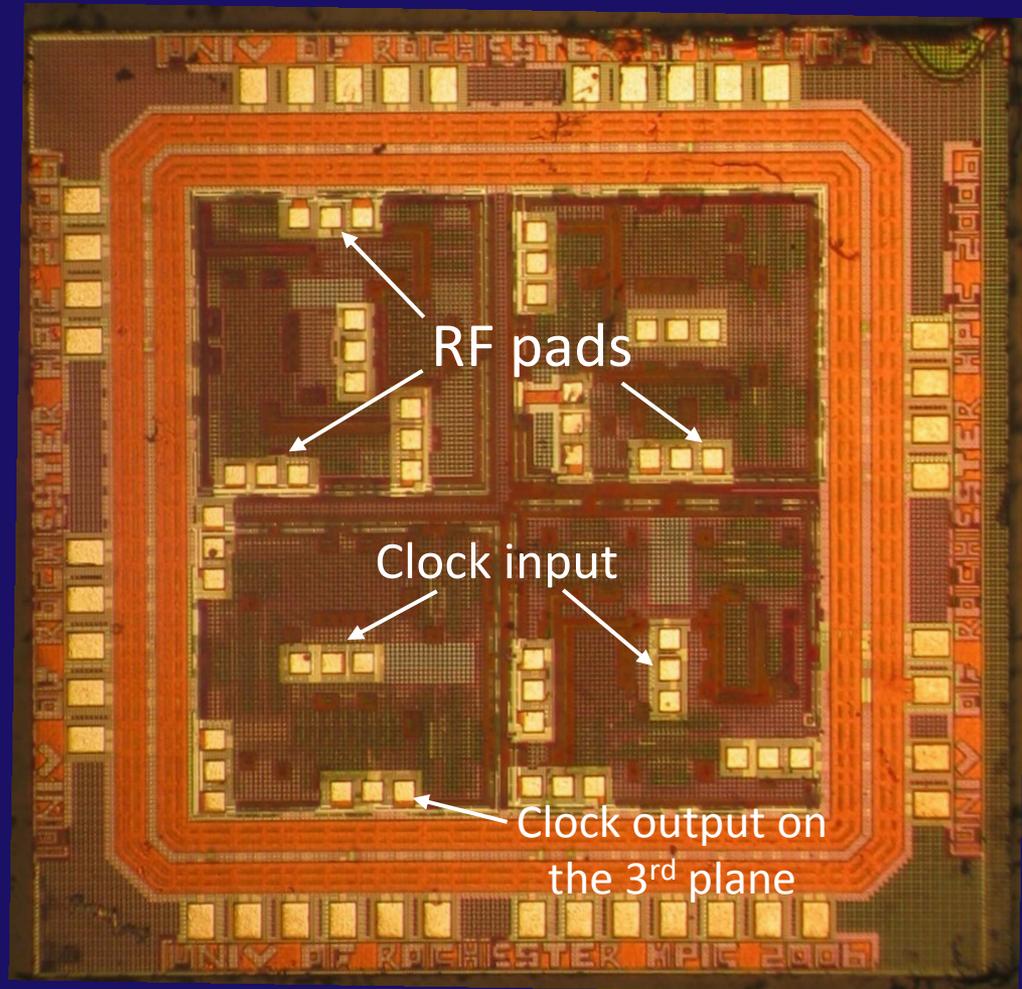
- The clock network on the 2<sup>nd</sup> plane is rotated by 90° to eliminate inductive coupling

# Fabricated 3-D Test Circuit

RF probe

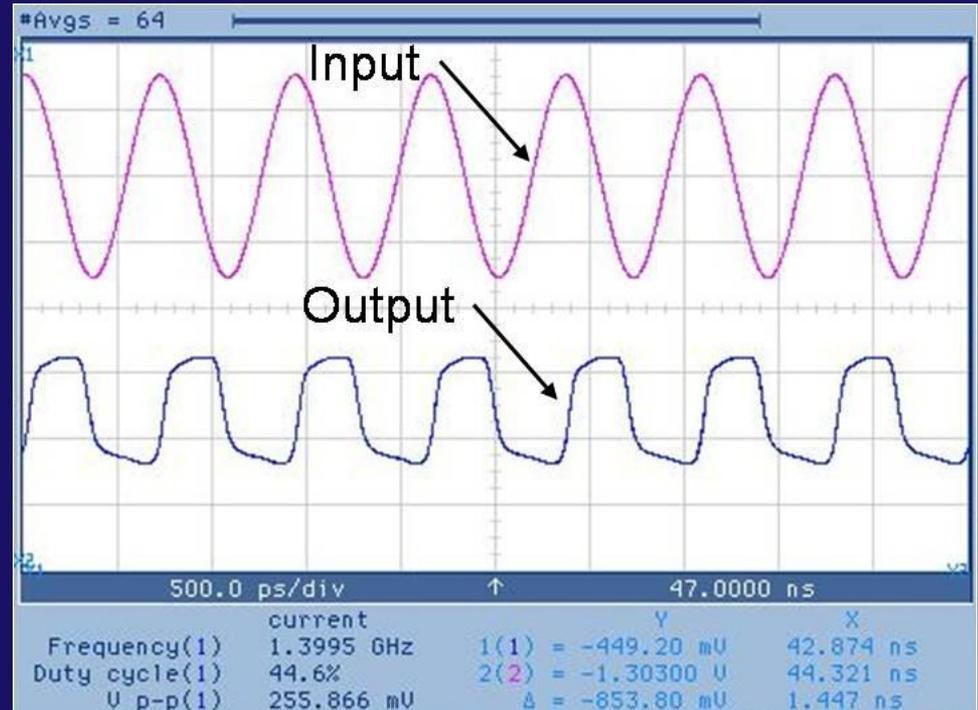
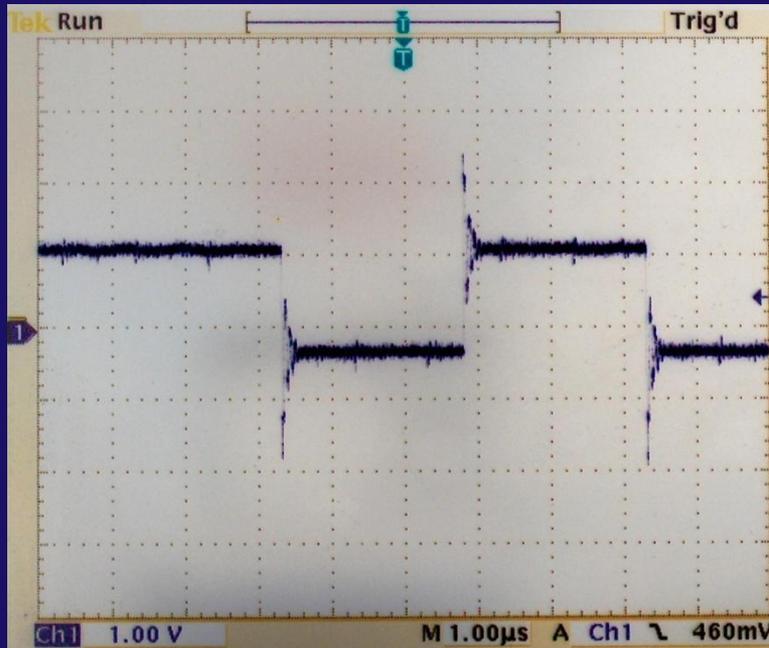


Decoupling capacitor



- Full custom design
- ~120K transistors

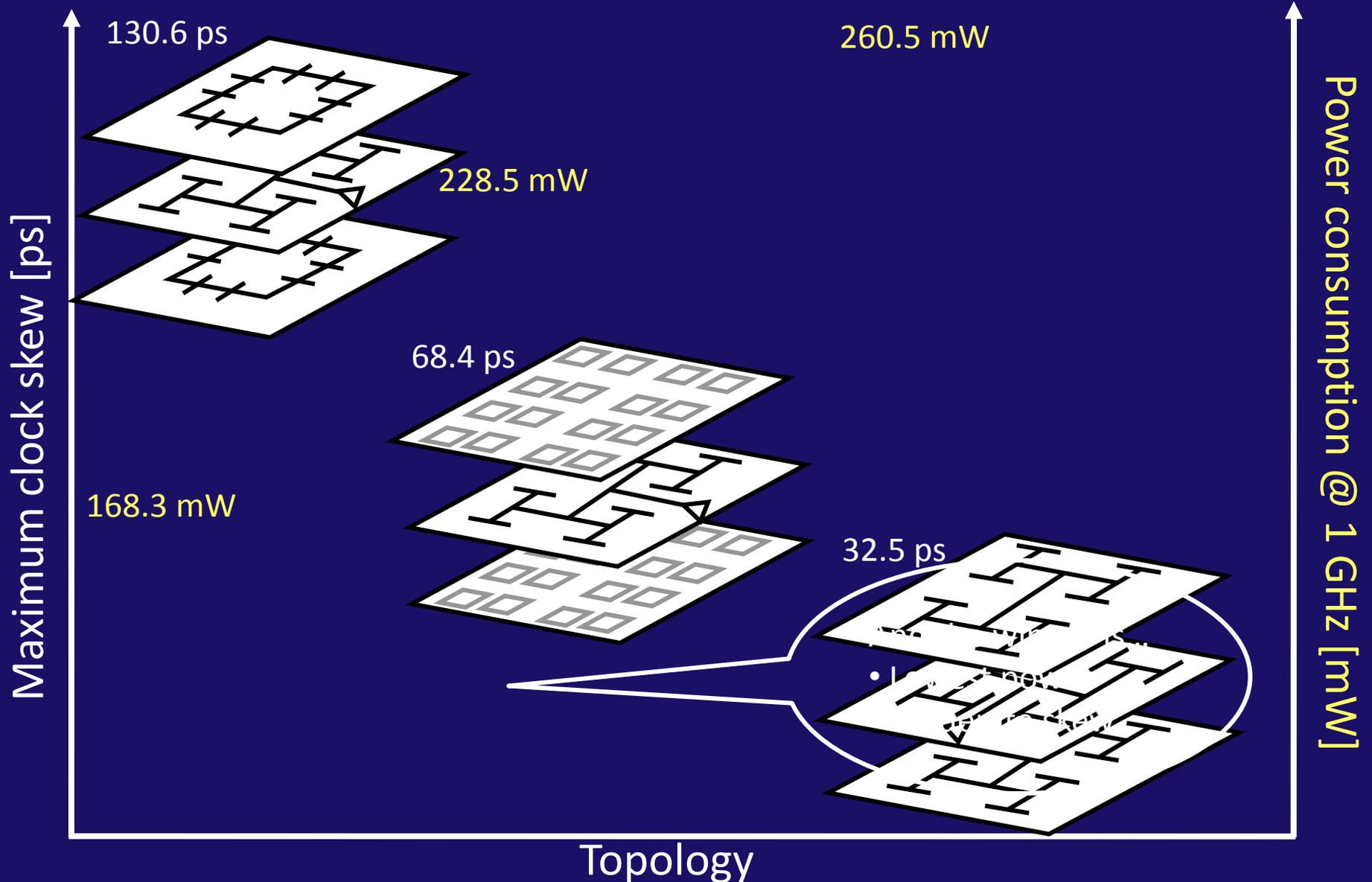
# Clock and Data Waveforms



- Output bit at 1 MHz

- Clock output at 1.4 GHz from the 3<sup>rd</sup> plane

# Clock Skew and Power Measurements



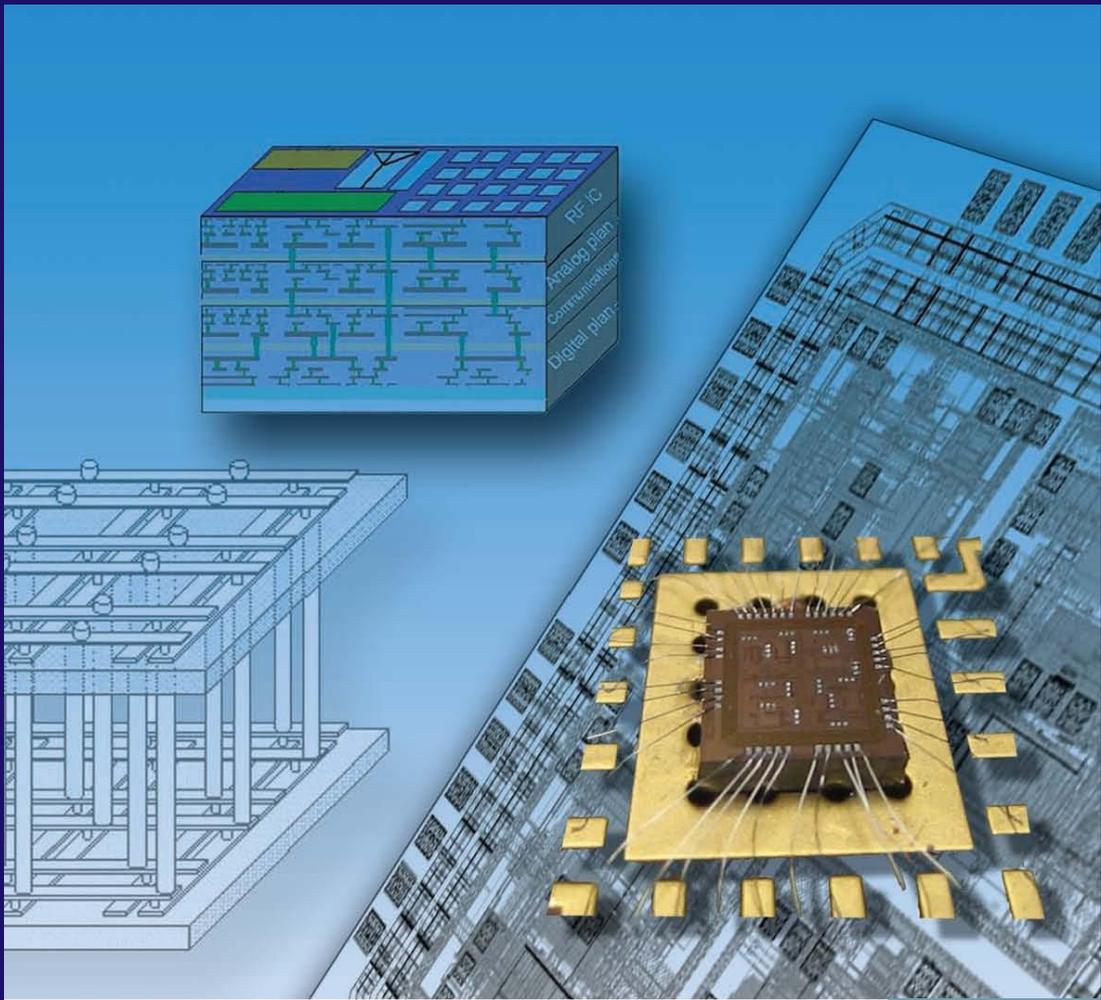
\*V. F. Pavlidis, I. Savidis, and E. G. Friedman, "Clock Distribution Networks for 3-D ICs," *Proceedings of the IEEE International Conference of Custom Integrated Circuits and Systems*, September 2008

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# Conclusions

- Three-dimensional integration is a promising interconnect paradigm for future ICs
- Efficient and accurate techniques are required for modeling and placing interplane vias
- 3-D NoC topologies exhibit significant power and speed advantages
- A 3-D circuit operating at 1.4 GHz has been designed, fabricated, and measured
- 3-D integration is a likely next step in the evolution of semiconductor technology



# THREE-DIMENSIONAL INTEGRATED CIRCUIT DESIGN

VASILIS F. PAVLIDIS EBY G. FRIEDMAN

